REMARKS

Summary of Claim Status

Claims 26-37 are pending in the present application after entry of the present amendment. Claims 26-37 are rejected for the reasons discussed below. Applicants respectfully request favorable reconsideration of the claims and withdrawal of the pending rejections and objections in view of the present amendment and in light of the following discussion.

Rejections Under 35 U.S.C. § 102

Claims 26-28 and 32-34 are rejected under 35 U.S.C. § 102(e) as being anticipated by Sani et al., U.S. Patent Application Publication No. US 2003/0218478 A1 ("Sani"). Applicants thank the Examiner for an explicit and clear description of how Sani is being read. Applicants, however, respectfully traverse this rejection as to all claims

Applicants have amended Claim 26 to recite a programmable logic device comprising a plurality of resources logically subdivided into a plurality of programmable logic blocks. The amendment is fully supported by the specification as filed, for example at ¶ [0021] of the specification. Claim 26 further recites a plurality of first switch elements, wherein each first switch element is coupled between one of the programmable logic blocks and a first voltage supply terminal. Applicants respectfully submit that Sani does not teach or even suggest at least these features.

First, Sani does not teach or even suggest a plurality of programmable logic blocks. The Examiner identifies element 210 of Sani as corresponding to a plurality of programmable logic blocks. However, element 210 is actually described in Sani to be "a logic gate," "logic gates," or "LVT [low voltage threshold] logic gates." See, e.g., Sani at p. 2, ¶¶ [0029] – [0031]. Notably, nowhere is it even mentioned, much less taught or disclosed, in Sani that a plurality of such elements may exist. That is, Sani only discloses a single element 210, and not a plurality.

Moreover, Sani does not teach a plurality of resources logically subdivided into a plurality of programmable logic blocks. In fact, Sani does not even mention logical subdivision of resources, or any similar concept. As noted above, Sani merely describes a single element 210 coupled between a headswitch and a footswitch. In Figs. 4 and 6, Sani shows examples of element 210 comprising a single CMOS inverter. Thus, since Sani only discloses a single element 210, it would be impossible for Sani to teach a plurality of resources logically subdivided into a plurality of programmable logic blocks as claimed by Applicants. Likewise, again since Sani only discloses a single element 210 coupled to a single headswitch 212, it would be impossible for Sani to teach a plurality of first switch elements, wherein each first switch element is coupled between one of the programmable logic blocks and a first voltage supply terminal.

Therefore, for at least the foregoing reasons, Applicants believe Claim 26 is allowable, and allowance of Claim 26 is respectfully requested.

Claims 27, 28, and 32 depend from Claim 26, and thus include all of the limitations of Claim 26. Applicants believe Claim 26 is allowable for the reasons set forth above. Therefore, Applicants believe Claims 27, 28, and 32 are also allowable for at least the same reasons, and respectfully request allowance of Claims 27, 28, and 32.

Claim 33 recites a plurality of programmable logic blocks and a plurality of voltage regulators, wherein each voltage regulator is coupled between one of the programmable logic blocks and a first voltage supply terminal. Applicants respectfully submit that Sani does not teach or disclose at least these features. First, as explained above, Sani does not disclose a plurality of programmable logic blocks. Sani merely discloses a single element 210, and does not teach or even suggest a plurality of programmable logic blocks as recited in Claim 33.

Furthermore, Sani does not even mention, much less teach or suggest, a voltage regulator, or any similar concept. Sani merely discloses a headswitch 212 and a footswitch 214, where headswitch 212 is a high voltage threshold PMOS transistor, and footswitch 214 is a high voltage threshold NMOS transistor. See, e.g., Sani at p.

2, ¶¶ [0029] – [0030]. As is known to those of ordinary skill in the art, a headswitch or a footswitch is not a voltage regulator. For instance, the specification describes an example of a regulator that can be controlled to provide either a full voltage or a reduced voltage. See, e.g., Specification at pp. 8-9, ¶ [0033]. As noted in the specification, this may desirable, for example, to maintain the state of the associated blocks. Id. Sani merely teaches the use of a headswitch/footswitch, and does not teach or disclose any regulator.

Therefore, for at least the foregoing reasons, Applicants believe Claim 33 is allowable, and allowance of Claim 33 is respectfully requested.

Claim 34 depends from Claim 33, and thus includes all of the limitations of Claim 33. Applicants believe Claim 33 is allowable for the reasons set forth above. Therefore, Applicants believe Claim 34 is also allowable for at least the same reasons, and respectfully request allowance of Claim 34.

Rejections Under 35 U.S.C. § 103

Claims 29-31 and 35-37 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Sani in view of Goetting et al., U.S. Patent No. 5,958,026 ("Goetting"). Applicants respectfully disagree and traverse the rejection as to all claims.

Claims 29-31 depend from Claim 26, and thus include all of the limitations of Claim 26. Applicants believe Claim 26 is allowable for the reasons set forth above. Therefore, Applicants believe Claims 29-31 are also allowable for at least the same reasons. Claims 35-37 depend from Claim 33, and thus include all of the limitations of Claim 33. Applicants believe Claim 33 is allowable for the reasons set forth above. Therefore, Applicants believe Claims 35-37 are also allowable for at least the same reasons.

Moreover, *prima facie* obviousness has not been established, which requires some suggestion or motivation to modify or combine reference teachings. See, e.g., MPEP § 2142. In this case, the Examiner stated "it would have been obvious to one of ordinary skill in the art at the time of applicant's invention to have provided the circuit

of Sani with control circuit as taught by Goetting in order to provide configuration data and enable/disable signal to the control circuit." Office Action at p. 4. Applicants respectfully submit it would not have been obvious to combine Sani and Goetting in the manner suggested by the Examiner. Sani relates to a circuit having a sleep mode having an output for preventing crowbar current. See, e.g., Sani at Abstract. In contrast, Goetting discloses an input/output buffer for an FPGA that van be configured to comply with multiple I/O standards. See, e.g. Goetting at Abstract. Thus, Sani is directed to preventing crowbar current, whereas Goetting is directed to an I/O buffer. It would not have been obvious to apply the control circuit of an I/O buffer in Goetting to a circuit with a sleep mode of Sani. In fact, nowhere in Sani is it suggested that any configuration data is necessary or desirable for providing the sleep signal.

Furthermore, the control circuit of Goetting is used to configure variously-sized pullups and pulldowns for different I/O standards. See, e.g., Goetting at col. 5, lines 10-46. In contrast, the headswitch and footswitch of Sani are used to reduce the leakage current responsive to a sleep signal. No actual control circuit for providing the sleep signal is disclosed in Sani. Thus, the headswitch and footswitch of Sani are controlled by a sleep signal generated by some implicit circuit for placing the circuit in a sleep or stand-by mode, and not to configure an I/O buffer as disclosed in Goetting. Therefore, it would not have been obvious for one of ordinary skill to combine Sani and Goetting, and *prima facie* obviousness has not been established.

For at least the foregoing reasons, Applicants respectfully request allowance of Claims 29-31 and 35-37.

Conclusion

No new matter has been introduced by any of the above amendments. In light of the above amendments and remarks, Applicants believes that Claims 26-37 are in condition for allowance, and allowance of the application is therefore requested. If action other than allowance is contemplated by the Examiner, the Examiner is respectfully requested to telephone Applicants' attorney, Justin Liu, at 408-879-4641.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Commissioner for Patents, P.O. BOX 1450, Alexandria, VA 22313-1450, on May 16, 2005.

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Signature